REMARKS

Claims 1-30 are pending. Applicants respectfully request reconsideration and reexamination of the application.

Applicants note that the Office Action Summary (Office Action, pg. 1) lists Claims 1-30 as rejected. However, in the Allowable Subject Matter section (Office Action, pg. 4), Claims 13-16 are noted as allowed by Examiner. Applicants believe that Claims 13-16 were allowed by Examiner, however, Applicants are not clear of the status of at least Claims 4-8, 12, 19, 22, 24, or 30 as these claims were neither cited in a rejection nor objected to by Examiner. Applicants believe that all of the claims are in condition for allowance based on this response to the Office Action. However, if a subsequent Office Action is submitted, Applicants request that the Examiner's position with respect to all of the claims be set forth as required under MPEP §707 so that Applicants are provided with a fair opportunity to respond.

Claims 1-3, 9-11, 17, 18, 20, and 26-29 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,622,208 to North [herein referred to as "North"] in view of U.S. Patent No. 6,741,846 to Welland et al. [herein referred to as "Welland"].

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Examiner admits that North does not disclose that the input signals have a possible range of voltage levels and signal types, but cites Welland as disclosing a first circuit (204) adapted to programmably receive an input signal having a possible range of voltage levels and signal types (Office Action pg. 3). Applicants respectfully disagree as Welland disclosed that first circuit 204 is simply a divide-by-R counter (col. 6, lns. 35-42). Thus, first circuit 204 of Welland is approximately the same as prescaler 906 of North, which was discussed and distinguished in the prior Office Action response.

Furthermore, Welland (at col. 26, lns. 56-58 as cited by Examiner) only recites that "[t]he technique described herein to provide a plurality of signals for the phase detector/sample hold circuit 1502 is useful over a wide range of applications, including the generation of high frequency signals for wireless telephones." Applicants respectfully submit that the plurality of signals to phase detector/sample hold circuit 1502 (e.g., in Fig. 16) are provided by conventional dividers (e.g., blocks 1550, 214, and 204) and is not relevant to what is recited in the present claims.

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Specifically, North alone or in combination with Welland fails to teach or suggest "a first circuit adapted to programmably receive an input signal, having a possible range

of voltage levels and signal types" as recited in Claim 1, "receiving an input signal, wherein the input signal may be a single-ended signal type or a differential signal type" as recited in Claim 17, or "programmably receiving input signals of various signal types and voltage levels and generating an input signal for a phase-locked loop" as recited in Claim 26.

Therefore, Applicants respectfully submit that Claims 1, 17, and 26 patentably distinguish over North in view of Welland and that corresponding dependent Claims 2, 3, 9-11, 18, 20, and 27-29 are also distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claims 1-3, 9-11, 17, 18, 20, and 26-29 be withdrawn.

Claims 21, 23, 25, 26, and 28 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,690,224 to Moore [herein referred to as "Moore"] in view of Welland.

As noted above, Welland discloses that first circuit 204 is simply a divide-by-R counter (col. 6, lns. 35-42). Applicants respectfully submit that Welland fails to cure the deficiencies as noted in the prior Office Action response, with Moore disclosing multiplexer block 222 receiving and providing one of the standard reference clock signals to PLL 200.

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Specifically, Moore alone or in combination with Welland fails to teach or disclose "an input circuit programmable to receive input signals of various signal types and voltage levels" as recited in Claim 21 or "programmably receiving input signals of various signal types and voltage levels and generating an input signal for a phase-locked loop" as recited in Claim 26.

Therefore, Applicants respectfully submit that Claims 21 and 26 patentably distinguish over Moore in view of Welland and that corresponding dependent Claims 23, 25, and 28 are also distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claims 21, 23, 25, 26, and 28 be withdrawn.

Accordingly, Applicants respectfully submit that Claims 1-30 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

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If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Commissioner for Patents, Fax No. 703-872-9306 on the date stated below.

Tina Kavanaugh March 28, 2005

Respectfully submitted,

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